High Efficiency CMOS Class E Power Amplifier for Bluetooth

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ABSTRACT

A power amplifier for wireless application has been implemented in a standard 0.25-um CMOS technology. The power amplifier employs class-E topology to exploit its soft-switching property for high efficiency [1]. The dc-feed inductance in the class-E load network allows the load resistance to be larger for the same output power than RF choke. The input waveform of class-E power amplifier is generated by driver stage of class-F to turn the power transistor on and off. By employing these design techniques, the simulated results shows that the power amplifier can deliver 21dbm output power to 50-Ω load at 2.4GHz for Bluetooth with 47% power-added efficiency(PAE) from a 2.5-V supply without stressing the active devices.

1. INTRODUCTION

Traditionally CMOS technology is confined to the digital and baseband part of radio transceiver. But it is a competition technology for RF front-end due to the progress in the last few years. The CMOS RF transceiver also expands its application area to radio system with requirement. A single chip CMOS radio has been arousing interest for low-cost and low-power portable radio device though it is still researched and estimated its feasibility to combine the RF front-end with the rest of the mobile terminal on the same die. Even the less ambitious objective of implementing the mobile terminal in a set of separate chips in the same CMOS technology may bring considerable economic benefits, however, as it enables a company to rationalize the number of different technologies that have to be maintained for a given product. In this spirit, the feasibility of realizing efficient power amplifiers in regular CMOS technology is also beginning to receive increased attention [2].

The basic class-E circuit is shown in Fig.1. The transistor is connected with the Radio Frequency Choke (RFC) to the supply voltage and to the load network, which is made up a capacitor C shunting includes the transistor output capacitor and external capacitor C1 in parallel with it. C2 and L1 are series resonant circuit. The class-E power amplifier is a non-linear power amplifier and the transistor works like to switch [3], so that has high power added-efficiency (PAE) and high efficiency.

Therefore this paper describes a 2.4GHz power amplifier in a 0.25-um CMOS technology and class-E power amplifier structure.

2.CIRCUIT STRUCTURE AND DESIGN

2.1 Design Method

In this quoted circuit structure of the power amplifier, the class-F stage could generate square waveform to drive the class-E stage. It will reduce the power loss in the transistor [4].

Because the ideal switch does not have an overlapping period of nonzero switch voltage and current, the class-E stage would assume a role of this.

2.2 Driver Stage Design

The basic ideal class-F stage is used to shape the output signal at the drain of the transistor such that it has more square shape than a sinusoidal shape [5]. The load network provides a high termination impedance at the first and third harmonics, thus the voltage waveform across the switch exhibits sharper edges than sinusoid, thereby lowering the power loss in the transistor. Fig. 2 shows a class-F topology and drain waveform of the transistor. The tanks consisting of L1, C1 and L2, C2 resonate at f_{in} and $3f_{in}$, respectively, and boost the first and third harmonics at drain of the transistor. Thus, the voltage across the switch approaches a rectangular waveform as the third harmonic becomes stronger.

2.3 Full Circuit Design

Fig. 3 shows the full circuit diagram, and it is designed for Bluetooth in 0.25-um CMOS technology. It consists of a class-F driver stage and class-E power stage.

The class-E power stage use an interdigitated TSMC NMOS model with a total width of 960-um and 3*32 fingers as the switch. A larger transistor has lower on-resistance (r_{on}) of an NMOS switch and higher output current. And lower on-resistance (r_{on}) has higher efficiency. Load resistance R_L and on-resistance (r_{on}) of an NMOS switch per unit channel width, and the radio r_{on} / R_L are shown the channel length L_{min}. The drain efficiency can be calculate from [2]

$$DE = \frac{1}{1 + 1.4 \times (\frac{r_{on}}{RL})} \qquad (1)$$

The class-F driver stage use an interdigitated TSMC NMOS model with a total width of 240-um and 8 finger add 16 finger, two parallel tune LC circuits resonating at the first and third harmonics of input frequency and input match network. Maximum drain voltage occurs when $\theta = 2\tan^{-1}(2/\pi)$ [6]

$$Vd, \max = 2\pi VDD \tan^{-1}(\frac{2}{\pi}) = 3.562VDD \qquad (2)$$

Because breakdown voltage of CMOS devices is very low, base on the theory, the maximum drain voltage of class-E approximate 3.562×VDD, as is the case for an ideal class-E power amplifier with an RF choke. At a limited efficiency of 50%-60% or less for practical class-E power amplifier, the peak drain voltage stress can be as low as 3.562×0.6×VDD, 0.6 is attenuation factor of circuit. The breakdown voltage of CMOS 0.25-um device approximate 5.4V [7], and this design use 2.5V supply voltage so Vd = 3.562×0.6×2.5 = 5.343V. For this reason, the circuit does not breakdown.

The dc-feed inductor (L_{dc}) can either be an RF choke or finite inductance. One method to provide the relief on the supply voltage and the load resistance is to use a finite inductance instead of RF choke. The passive elements (L6, L7, C8, C9) of output are external components. L6 and L7 use bonding wire, because bonding wire have high quality factor (Q). C8 and C9 use lump components.

3. SIMULATION RESULT

3.1 Waveform Simulation

The circuit is simulated in TSMC CMOS 0.25-um technology with ADS. The simulated results of drain voltage waveform and drain current waveform of power stage transistor are shown in Fig.4.

Fig. 5 shows voltage and current waveform of output. The output peak voltage is 3.843V and output peak current is 76.86mA. The power amplifier could supply 21dBm output power.

3.2 S-Parameter Simulation

Fig. 6 is input reflection coefficient, reverse transmission coefficient and forward transmission coefficient. S_{11} of the circuit is approximate -20dB at 2.4GHz. Therefore input return loss is lower. S_{12} of the circuit is approximate –31dB at 2.4GHz. Therefore isolation of the circuit is best. S_{21} of the circuit is approximate 13.67dB at 2.4GHz.

3.3 Stability

The K-factor stability definition is used to identify whether the RF circuit oscillate, but the K factor is not used in the case of class-E power amplifier. Because the K factor is based on small signal analysis, however the class-E power amplifier is a nonlinear large signal power amplifier and transistor acting as a switch. Therefore the K factor is not used to determine the oscillation of the class-E power amplifier. The practical way to test stability in this case is to perform transient analysis and check the stability of the circuit [6]. Fig. 7 shows transient analysis diagram and indicates a stable result.

3.4 Performance Simulation

Fig. 8 shows transducer power gain and output power related with input power. When input power is 5dBm, the maximum transducer power gain is approximate 15.262dB.

Fig. 9 shows power added efficiency (PAE) and output power related with input power. The maximum PAE is 47.54%, when input power is 8 dBm. Table 1 shows some performance with different input RF power at 2.4GHz. The specification of the circuit is listed in Table 2.

$$PAE = \frac{Pout - Pin}{Pdc} \qquad (3)$$

3.5 Layout Consideration & Diagram

Ground inductance could affect both the efficiency and gain of the power amplifier. To solve this problem, we would increase the parallel bond wire on ground pads in the layout. Fig.10 shows the layout diagram of this circuit.

4. CONCLUSION

In this paper, we use low-cost CMOS process to design a class-E power amplifier with high efficiency for Bluetooth. The power amplifier structure use class-F driver stage to drive class-E power stage. The class-F stage could generate square waveform, and it would reduce power loss in transistor of class-E power amplifier. The simulation result shows the power amplifier can deliver 21dBm output power to 50-Ω load and 15dB transducer power gain at 2.4GHz with 47% PAE from 2.5 supply voltage.

5. REFERENCES

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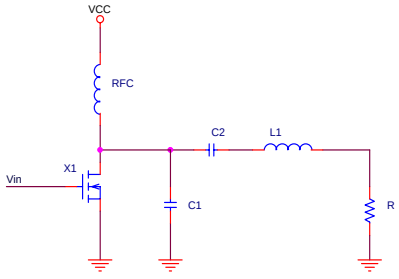

Fig.1 Class-E power amplifier

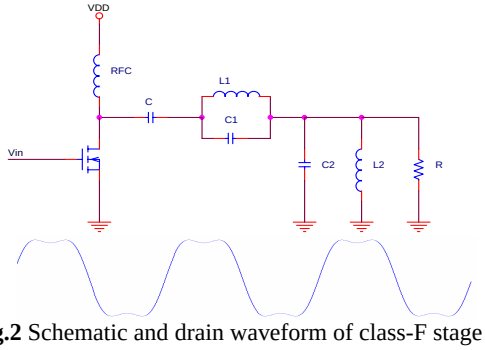

Fig.2 Schematic and drain waveform of class-F stage

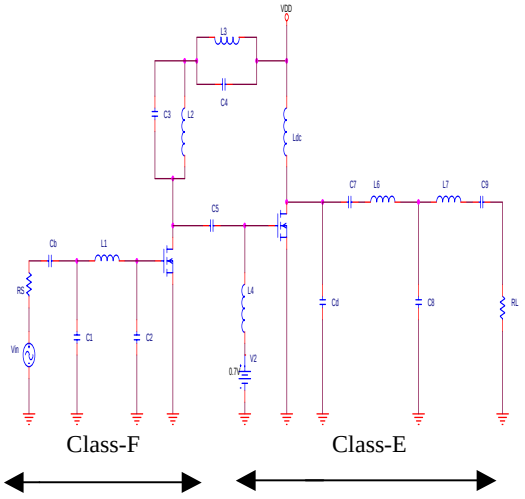

Fig.3 Circuit diagram of class-F driver and class-E power amplifier

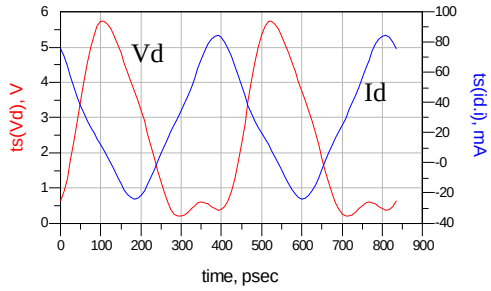

Fig. 4 The drain voltage and drain current waveforms of power stage

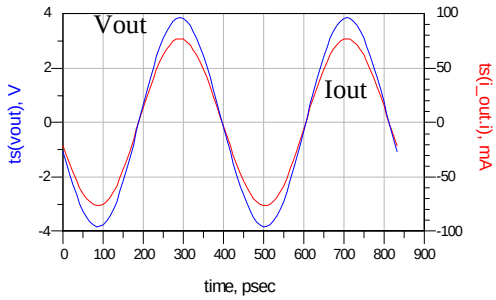

Fig.5 The output voltage and output current waveforms of power stage

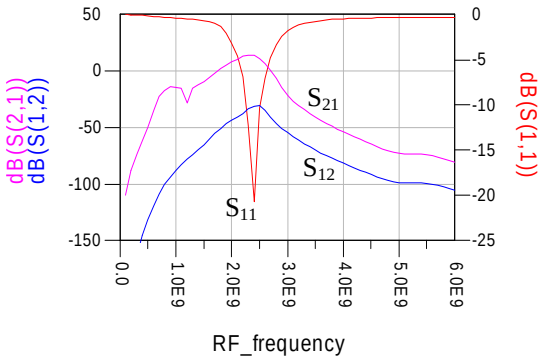

Fig. 6 S-Parameter Simulation

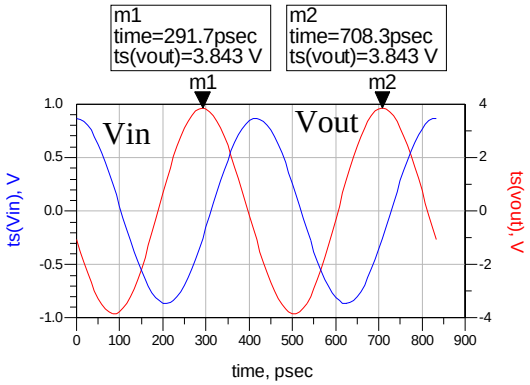

Fig.7 Input voltage and output transient analysis

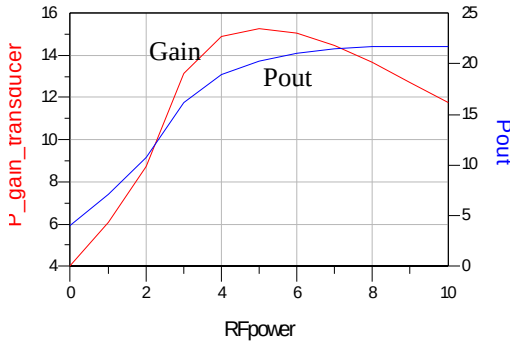

Fig. 8 Input power versus output power and transducer power gain

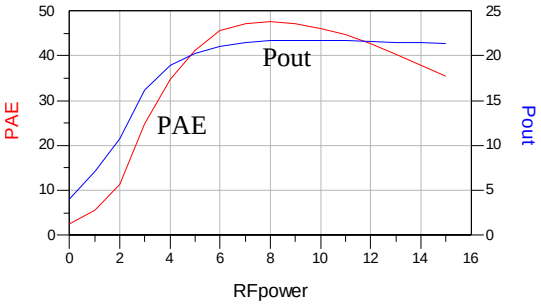

Fig.9 Input power versus output power and PAE

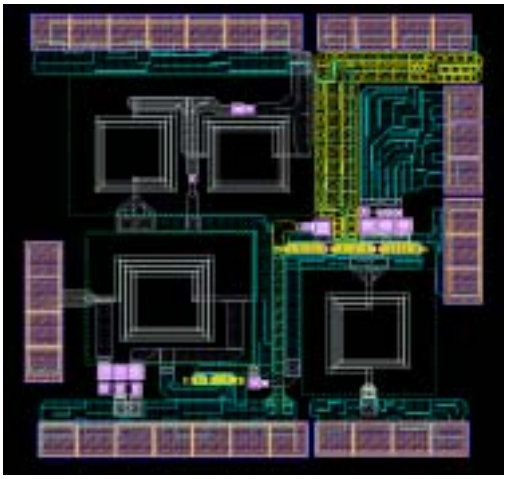

Fig.10 Layout diagram

Table 1

RFpower	Pout	PAE	Efficiency
0.000	4.010	2.446	4.057
1.000	7.070	5.503	7.310
2.000	10.717	11.358	13.121
3.000	16.157	24.849	26.112
4.000	18.914	34.793	35.953
5.000	20.262	41.265	42.531
6.000	21.070	45.526	46.989
7.000	21.486	47.255	49.000
8.000	21.671	47.540	49.674
9.000	21.737	47.069	49.716
10.000	21.746	46.122	49.430

Table 2

PA operating type	Class-E PA
Technology	CMOS 0.25-um
Frequency Range	2.4GHz
DC Supply	2.5V
Output power	>21dBm
Power Gain	>15dB
Efficiency (PAE)	>47%